In the Abstract:

Insert a new abstract as follows:

Low power delay test capabilities in Scan and Scan-BIST architectures occur by inserting a first cache bit memory between the scan input lead and the serial input to a first scan path segment. When the first segment is serially loaded, the last test bit remains in the first cache bit memory. When a last scan path segment is serially loaded and when the last bit is loaded into the last scan path segment, the last bit in the first cache bit memory is simultaneously loaded into the first scan path segment. This presents the desired stimulus signals to the logic circuits. The next clock signal to the scan path segments then captures the response from the logic circuits.